

## 100V N-Channel Enhancement Mode MOSFET

### Description

The 160N10 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V.

This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 160A$

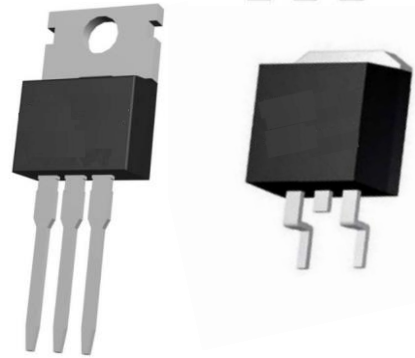
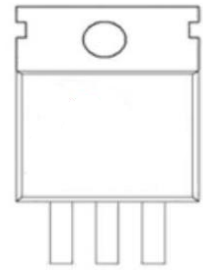
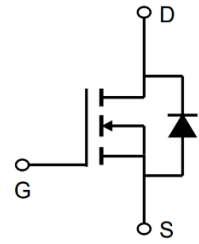
$R_{DS(ON)} < 4.2m\Omega$   $V_{GS} = 10V$  (Type:  $3.7m\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
VGS	Gate-Source Voltage	±20	V
ID@TC=25°C	Continuous Drain Current, VGS @ 10V	160	A
ID@TC=100°C	Continuous Drain Current, VGS @ 10V	105	A
IDM	Pulsed Drain Current	600	A
EAS	Single Pulse Avalanche Energy	540	mJ
IAS	Avalanche Current	60	A
PD @TC=25°C	Power dissipation	225	W
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
RθJA	Thermal Resistance Junction-Ambient	0.55	°C/W
RθJC	Thermal Resistance Junction-Case	62	°C/W

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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-source breakdown voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	110		V
VGS(th)	Gate threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA T <sub>J</sub> =25°C	2.5	3.0	4.2	V
IDSS	Zero gate voltage drain current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =25°C	-	-	1	μA
IDSS	Zero gate voltage drain current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =125°C	-	-	5	μA
IGSS	Gate-source leakage current	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V	-	-	100	nA
RDS(on)	Drain-source on-state resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =80A, T <sub>J</sub> =25°C	-	3.7	4.2	mΩ
gfs	Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =80A	-	130	-	S
Ciss	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz	-	3950	-	pF
Coss	Output Capacitance		-	1200	-	pF
Crss	Reverse Transfer Capacitance		-	45	-	pF
Q <sub>G</sub>	Gate Total Charge	T <sub>J</sub> =25°C, V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =80A	-	78	-	nC
Q <sub>gs</sub>	Gate-Source charge		-	32	-	nC
Q <sub>gd</sub>	Gate-Drain charge		-	17	-	nC
td(on)	Turn-on delay time	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =80A RG=5Ω	-	27	-	ns
t <sub>r</sub>	Rise time		-	52	-	ns
td(off)	Turn-off delay time		-	58	-	ns
t <sub>f</sub>	Fall time		-	23	-	ns
R <sub>G</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	-	0.77	-	Ω
VSD	Body Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>SD</sub> =50A	-	0.85	1.2	V
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	-	82	-	ns
Qrr	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	-	180	-	nC

#### Note :

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is VDD=82V, VGS =10V, L=0.1mH, IAS =53.8A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

### Typical Characteristics

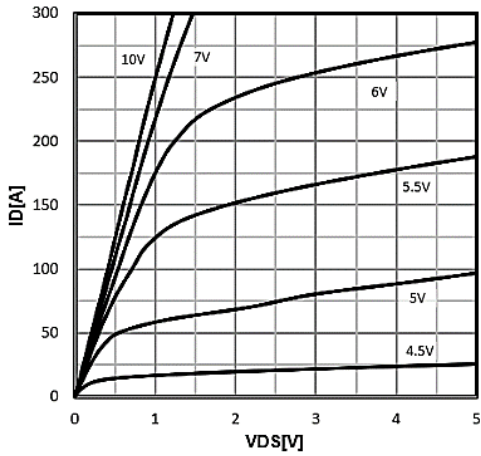


Figure 1. Type. Output Characteristics ( $T_j=25\text{ }^\circ\text{C}$ )

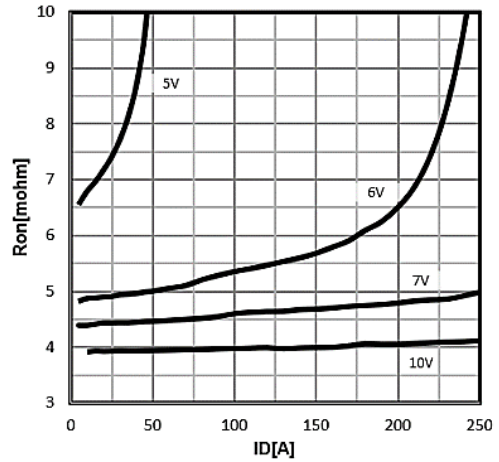


Figure 2. Type. drain-source on resistance

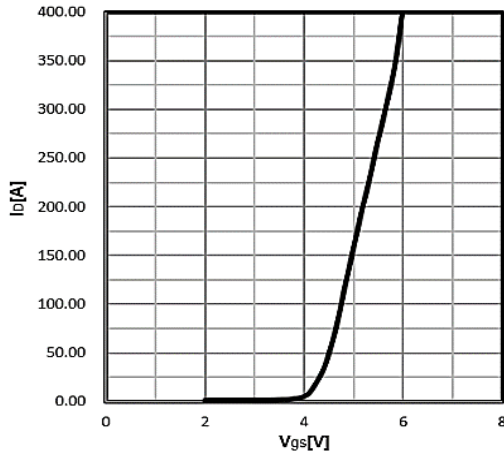


Figure 3. Type. transfer characteristics

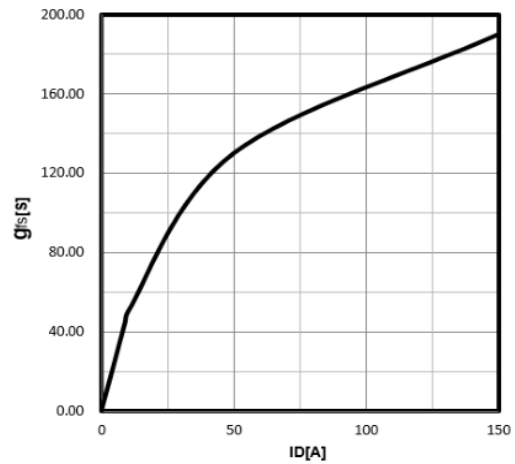


Figure 4. Type. forward transconductance

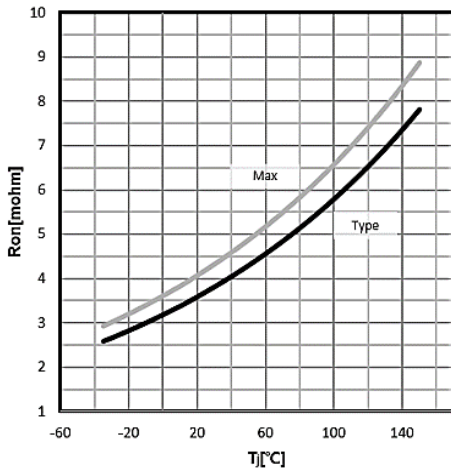


Figure 5. Drain-source on-state resistance  $R_{DS(on)} = f(T_j)$ ;  $I_D = 80\text{A}$ ;  $V_{GS} = 10\text{V}$

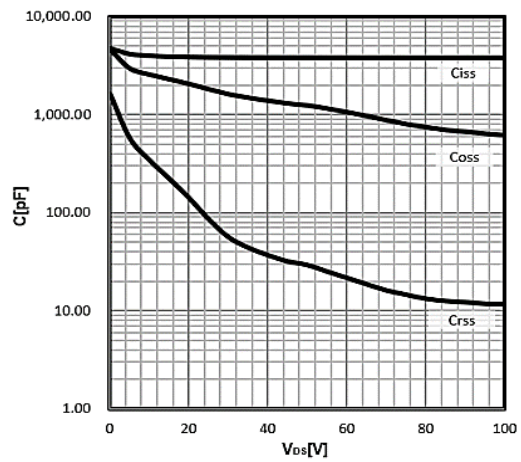


Figure 6. Body-Diode Characteristics  $C = f(V_{DS})$ ;  $V_{GS} = 0\text{V}$ ;  $f = 1\text{MHz}$

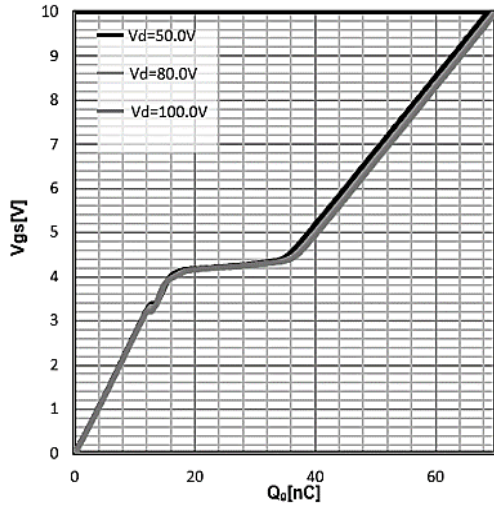
**100V N-Channel Enhancement Mode MOSFET**


Figure 7. Typ. gate charge  
 $V_{GS} = f(Q_{gate})$ ;  $I_D = 20A$

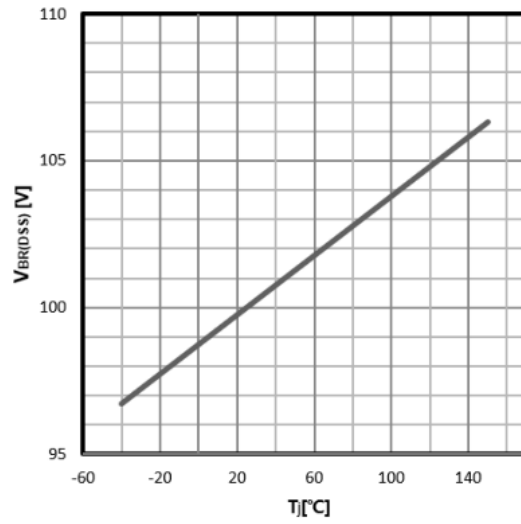


Figure 8. Drain Current Derating  
 $V_{BR(DSS)} = f(T_j)$ ;  $I_D = 250\mu A$

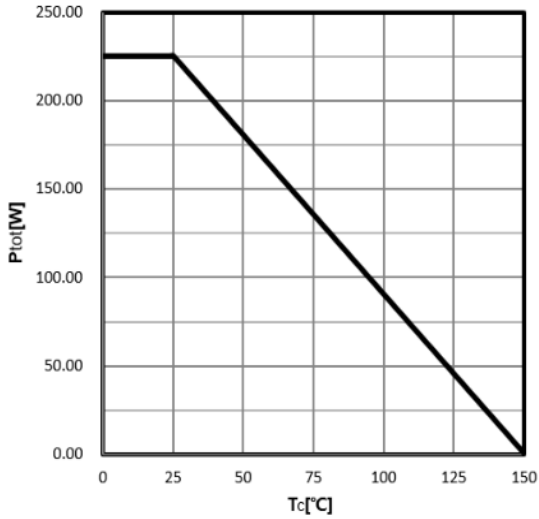


Figure 7. Power Dissipation

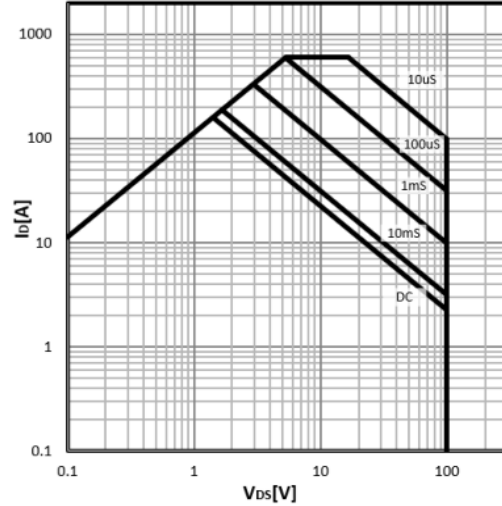


Figure 8. Safe operating area

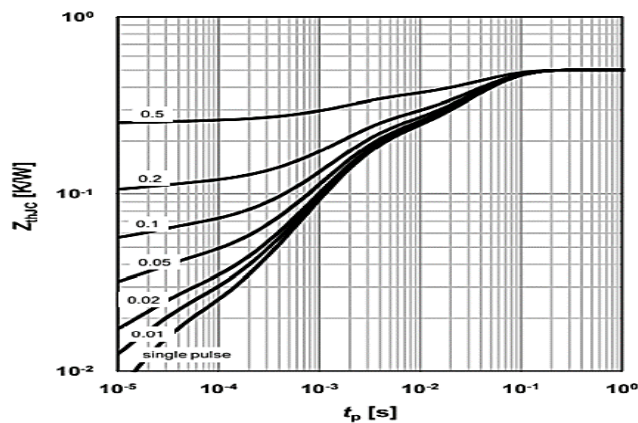
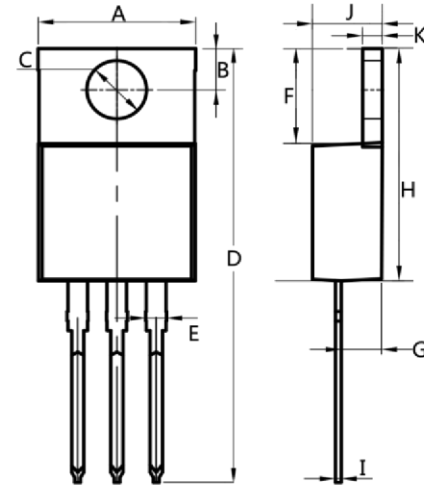


Figure 10. Max. transient thermal impedance

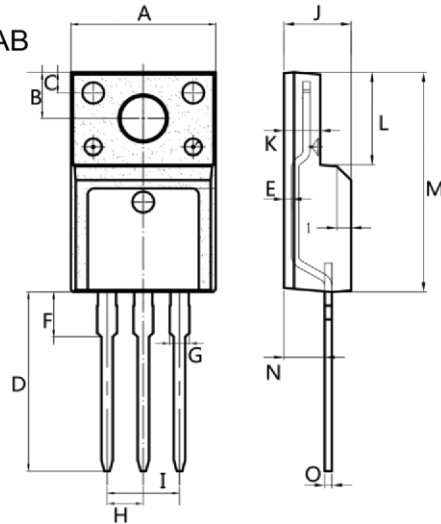
$$Z_{thJC} = f(t_p)$$

## 100V N-Channel Enhancement Mode MOSFET

**TO-220AB**


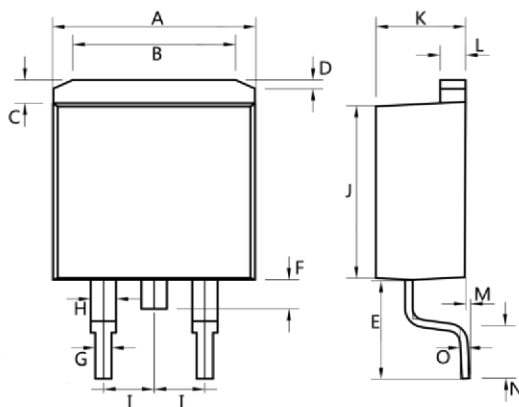
Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4

All Dimensions in millimeter

**ITO-220AB**


Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60

All Dimensions in millimeter

**TO-263**


Dim.	Min.	Max.
A	10.0	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45

All Dimensions in millimeter